Bonus Lecture #1: The FLP Impossibility Theorem

COMS 4995-001: The Science of Blockchains URL: https://timroughgarden.org/s25/

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Goals for Bonus Lecture #1

- 1. Understanding the asynchronous model.
	- what does "no assumptions on message delays" mean?
- 2. Proof of the FLP Theorem.
	- state machine replication (SMR) is "unsolvable" in asynchrony
	- need to compromise to make further progress
		- pull back to "partial synchrony" (see next lecture)
		- relax consistency guarantees (could be a good project)
		- randomized protocols that succeed with high probability
			- could also be a good project

SMR: Synchrony vs. Asynchrony

Lecture #3: in the synchronous model, can solve the SMR problem (i.e., via a consistent and live protocol), even with an arbitrary number of crash faults.

• uncrashed validators remain consistent, guarantee liveness

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Question: what's the "asynchronous model"?

- shared global clock, timesteps $0,1,2,...$
	- traditional asynchronous model does not have this (only makes today's impossibility result stronger)
- pool M of outstanding messages (sent but not yet received)

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	- 2. non-crashed validators decide which txs to finalize, messages to send
		- as instructed by whatever protocol they're running
		- messages sent injected directly into M

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- constraints on adversary:
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	- every message sent must eventually get delivered 10^{10}

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The FLP Impossibility Theorem

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Theorem: [FLP85] no SMR protocol guarantees consistency and liveness in the setup above.

• "input " = tx *a*, "input 1 " = tx *b* [each validator gets input 0 or 1]

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Assume [for contradiction]: protocol ∏ guarantees consistency and liveness in the preceding setup.

- "protocol" = specifies what validators should do in each timestep
	- as a function of their input, the timestep, and messages received
- think of ∏ as deterministic (or with adversary-controlled randomness)

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Consequences:

- 1. liveness of Π → every non-faulty validator eventually outputs 0 or 1
- 2. consistency of $\Pi \rightarrow$ all non-faulty validators eventually output the same thing
- 3. if all inputs are 0 (respectively, 1) \rightarrow all outputs are 0 (respectively, 1)

Configurations

Definition: a *configuration* C := the state of all validators and the message pool M at the beginning of a timestep.

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Note: strategy of adversary in a timestep (which messages to deliver, validator to crash) induces a transition $C \rightarrow C'$.

Proof plan: devise strategy of adversary resulting in an infinite sequence $C_0 \rightarrow C_1 \rightarrow C_2 \rightarrow C_3 \rightarrow \ldots$ of configurations such that no validator outputs in any C_t . [note: would contradict liveness]

Definition: a *benign adversary* always delivers all messages in the pool M and never crashes any validators.

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- note: by consequences (1)-(3) above, no other possibilities
	- (technically, defined only for configurations C with at most one crash)

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Next: define a "pivotal" configuration as (roughly) one in which crashing a validator flips the output of the protocol. $\qquad \qquad _{29}$

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	- as far as other validators j≠i can tell, i crashed at time t'
		- only difference is the state of M, which validators do not observe

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Definition: for an i-restricted configuration C, *val(C \ i)* := output of the protocol ∏ with an adversary that:

- at timesteps < t: behaves identically to the adversary in C (delivers same msgs each timestep) except it crashes i at t'
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Definition: for an i-restricted configuration C, $val(C \setminus i) :=$ output of the protocol Π with an adversary that:

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- at timesteps ≥ t: is benign

Definition: an i-restricted C is *i-pivotal* if val(C) \neq val(C \ i).

• key point: C pivotal \rightarrow no validators have output yet (why?) $_{35}$

An Infinite Sequence of Pivotal Configurations

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Recall proof plan: devise strategy of adversary resulting in an infinite sequence $C_0 \rightarrow C_1 \rightarrow C_2 \rightarrow C_3 \rightarrow \ldots$ of configurations such that no validator outputs in any C_t . [contradicts liveness]

- suffices to use only pivotal configurations
- we will exhibit such a sequence, inductively

• let X_i = initial configuration in which validators 1,2,..., i have input 1 and validators $i+1$, $i+2$, ..., n have input 0

– note: all X_i's j-restricted for all j [no crashes, M is empty]

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- note: for some $i \ge 1$, $val(X_{i-1})=0$ and $val(X_i)=1$
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	- if i crashes immediately, doesn't matter whether its input was 0 or 1
	- in general: if validator sees identical messages at every timestep in two different executions, will behave identically (including the same output)

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	- if i crashes immediately, doesn't matter whether its input was 0 or 1
- so: either (i) val $(X_{i-1} \setminus i) = 1$ (in which case X_{i-1} is i-pivotal) or (ii) val $(X_i \setminus i) = 0$ (in which case X_i is *i-pivotal*)
	- either way, we have our initial pivotal configuration C_0 $\hspace{1.5cm}$ \hs

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because C_t is i-pivotal $\smile_{\mathsf{val}}(C_t) \neq \mathsf{val}(C_t \setminus \mathsf{i})$ \rightarrow val(Y) = val(Y \ i) in harder case, Y is not i-pivotal $\overline{}$ you check: val($C_t \setminus i$), val(Y \ i) defined by the exact same execution [with adversary crashing i at t']

• upshot: $val(C_t) \neq val(Y)$, say $val(C_t) = 0$ and $val(Y) = 1$ ⁵²

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- so: either (i) val(Y_{r-1} \ j) = 1 (in which case Y_{r-1} is j-pivotal) or (ii) val($Y_r \setminus j$) = 0 (in which case Y_r is j-pivotal)
	- either way, we have our next pivotal configuration C_{t+1}

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- good news: never uses a crash fault (only the *threat* of a fault)
- bad news: not guaranteed to eventually deliver every message
	- problem: if for some t, $C_t \rightarrow C_{t+1} \rightarrow C_{t+2} \rightarrow \ldots$ are all i-pivotal configurations generated using the "easy case," i's messages never get delivered

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	- fix: modify adversary strategy to crash i at timestep t, act benign thereafter
		- other validators can't tell the difference, protocol behavior unchanged
		- now a valid adversary strategy \rightarrow contradicts liveness of Π ! \blacksquare

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- 3. Use randomized protocols, solve SMR with high probability.
	- rich academic literature on this topic 14